

A Nonvolatile Register with a Reference Load Sharing Scheme

Reduction in power consumption and area by minimizing the number of MTJ devices

Overview

Intermittent computing executes tasks as energy accumulates, enabling continuous edge computing under unstable, low-power energy harvesting conditions. Ensuring processing continuity before and after frequent power interruptions is essential. A nonvolatile logic circuit using nonvolatile registers allows internal state retention with only local data transfers, making it a promising option.

Conventional nonvolatile registers connect 1-bit memory circuits (nonvolatile flip-flops, NV-FFs) per bit, requiring two MTJ devices per bit, leading to significant area and energy overhead. This invention proposes the Reference-Load Sharing Scheme (RLSS), where 1-bit information is retained between an MTJ device and a reference MTJ device using a sequential backup-restore process. This reduces MTJ device count, shares circuit functions, and achieves 49% lower energy consumption and 34% area reduction, as confirmed by simulations.

Product Application

- ❑ Nonvolatile registers and nonvolatile flip-flops
- ❑ Intermittent computing and energy harvesting
- ❑ Reduction in power consumption of existing desktop and supercomputers

IP Data

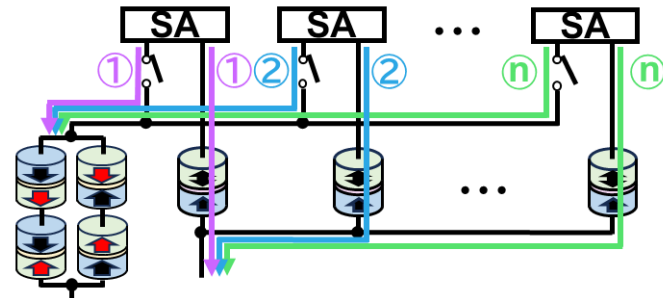
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Backup and Restore Operation and Performance Comparison

Conventional (NV-FF)



Reference-Load Sharing Scheme



	Conv.	RLSS
Area	×	○
Energy	×	○
Backup/Restore time	○	△

Related Works

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